

WHAT IS CLAIMED IS:

- 1 1. A semiconductor device, comprising:  
2 a dielectric pedestal located above and integral to a substrate and having first sidewalls;  
3 a channel region located above said dielectric pedestal and having second sidewalls; and  
4 source and drain regions opposing said channel region and each substantially spanning  
5 one of said second sidewalls.
- 1 2. The semiconductor device as recited in Claim 1 wherein said first and second sidewalls  
2 are substantially coincident.
- 1 3. The semiconductor device as recited in Claim 1 wherein each of said source and drain  
2 regions further substantially spans one of said first sidewalls.
- 1 4. The semiconductor device as recited in Claim 1 wherein said dielectric pedestal and said  
2 substrate comprise at least a portion of a silicon-on-insulator (SOI) substrate.
- 1 5. The semiconductor device as recited in Claim 1 wherein said channel region, said  
2 dielectric pedestal and said substrate comprise at least a portion of a silicon-on-insulator (SOI)  
3 substrate.
- 1 6. The semiconductor device as recited in Claim 1 wherein said dielectric pedestal is at least  
2 a portion of a buried oxide (BOX) layer located in said substrate.
- 1 7. The semiconductor device as recited in Claim 1 further comprising a silicide layer over at  
2 least portions of said source and drain regions.

1 8. The semiconductor device as recited in Claim 1 further comprising a gate structure  
2 including a gate oxide located above said channel region and a gate electrode located above said  
3 gate oxide.

1 9. The semiconductor device as recited in Claim 8 wherein said gate oxide has a thickness  
2 ranging between about 0.2 nm and about 2 nm.

1 10. The semiconductor device as recited in Claim 1 wherein said channel region has a length  
2 ranging between about 2 nm and about 100 nm.

3 11. The semiconductor device as recited in Claim 1 wherein said channel region has a  
4 thickness ranging between about 1 nm and about 20 nm.

1 12. A method of manufacturing a semiconductor device, comprising:  
2 providing a substrate having a channel layer located over a buried dielectric layer;  
3 forming a gate structure over said channel layer;  
4 removing portions of said channel layer and said buried dielectric layer using at least a  
5 portion of said gate structure as a mask, thereby defining a dielectric pedestal having first  
6 sidewalls and a channel region having second sidewalls; and  
7 forming source and drain regions opposing said channel region and each substantially  
8 spanning one of said second sidewalls.

1 13. The method as recited in Claim 12 wherein said first and second sidewalls are  
2 substantially coincident.

1 14. The method as recited in Claim 12 wherein each of said source and drain regions further  
2 substantially spans one of said first sidewalls.

1 15. The method as recited in Claim 12 wherein said providing a substrate includes providing  
2 a silicon-on-insulator (SOI) substrate.

1 16. The method as recited in Claim 12 further comprising forming a silicide layer over at  
2 least portions of said source and drain regions.

1 17. The method as recited in Claim 16 wherein said forming said silicide layer includes  
2 forming spacers opposing said gate structure and partially extending over said source and drain  
3 regions and employing said spacers as a mask.

1 18. The method as recited in Claim 12 wherein said forming said gate structure includes  
2 forming a gate oxide above said channel region and forming a gate electrode above said gate  
3 oxide.

1 19. The method as recited in Claim 18 wherein said gate oxide has a thickness ranging  
2 between about 0.2 nm and about 2 nm.

1 20. The method as recited in Claim 12 wherein said channel region has a length ranging  
2 between about 2 nm and about 100 nm.

1 21. The method as recited in Claim 12 wherein said channel region has a thickness ranging  
2 between about 1 nm and about 20 nm.

1 22. The method as recited in Claim 12 further comprising forming spacers on opposing sides  
2 of said gate structure, wherein said mask includes said spacers.

1 23. The method as recited in Claim 12 wherein said removing includes etching through said  
2 channel layer and at least partially into said buried dielectric layer.

1 24. The method as recited in Claim 12 wherein said forming said source and drain regions  
2 includes depositing one selected from the group consisting of:  
3 silicon;  
4 silicon-germanium; and  
5 polysilicon.

- 1 25. The method as recited in Claim 24 wherein said forming said source and drain regions
- 2 includes doping said one.

1     26.     An integrated circuit device, comprising:  
2             a semiconductor device, including:  
3                 a dielectric pedestal located above and integral to a substrate and having first  
4     sidewalls;  
5                 a channel region located above said dielectric pedestal and having second  
6     sidewalls; and  
7                 source and drain regions opposing said channel region and each substantially  
8     spanning one of said second sidewalls;  
9             an interlevel dielectric layer located over said semiconductor device; and  
10            vias spanning said interlevel dielectric layer and contacting said source and drain regions.

1     27.     The integrated circuit device as recited in Claim 26 wherein said first and second  
2     sidewalls are substantially coincident.

1     28.     The integrated circuit device as recited in Claim 26 wherein each of said source and drain  
2     regions further substantially spans one of said first sidewalls.

1     29.     The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal and  
2     said substrate form at least a portion of a silicon-on-insulator (SOI) substrate.

1     30.     The integrated circuit device as recited in Claim 26 wherein said channel region, said  
2     dielectric pedestal and said substrate form at least a portion of a silicon-on-insulator (SOI)  
3     substrate.

1 31. The integrated circuit device as recited in Claim 26 wherein said dielectric pedestal is at  
2 least a portion of a buried oxide (BOX) layer located in said substrate.

1 32. The integrated circuit device as recited in Claim 26 wherein said semiconductor device  
2 includes a silicide layer over at least portions of said source and drain regions.

1 33. The integrated circuit device as recited in Claim 26 wherein said semiconductor device  
2 includes a gate structure having a gate oxide located above said channel region and a gate  
3 electrode located above said gate oxide.

1 34. The integrated circuit device as recited in Claim 33 wherein said gate oxide has a  
2 thickness ranging between about 0.2 nm and about 2 nm.

1 35. The integrated circuit device as recited in Claim 26 wherein said channel region has a  
2 length ranging between about 2 nm and about 100 nm.

1 36. The integrated circuit device as recited in Claim 26 wherein said channel region has a  
2 thickness ranging between about 1 nm and about 20 nm.